2.2-V to 36-V, microPower Comparator

Check for Samples: TLV1701, TLV1702, TLV1704

FEATURES

- **Supply Range:**
  +2.2 V to +36 V or ±1.1 V to ±18 V
- **Low Quiescent Current:**
  55 µA per Comparator
- **Input Common-Mode Range Includes Both Rails**
- **Low Propagation Delay: 780 ns**
- **Low Input Offset Voltage: 300 µV**
- **Open Collector Outputs**
- **Industrial Temperature Range:**
  –40°C to +125°C
- **Small Packages:**
  - **Single: SC70-5, SOT23-5, SOT553-5**
  - **Dual: MSOP-8, QFN-8**
  - **Quad: TSSOP-14**

APPLICATIONS

- **Over and Undervoltage Detectors**
- **Window Comparators**
- **Over-Current Detectors**
- **Zero-Crossing Detectors**
- **System Monitoring for:**
  - **Power Supplies**
  - **White Goods**
  - **Industrial Sensors**
  - **Automotive**
  - **Medical**

DESCRIPTION

The TLV170x family of devices offers a wide supply range, rail-to-rail inputs, low quiescent current and low propagation delay. All these features come in industry standard, extremely-small packages, making these devices the best general-purpose comparators available.

These devices are available in single (TLV1701), dual (TLV1702 (1)) and quad (TLV1704) channel versions. Low input offset voltage, low input bias currents, low supply current, and open-collector configuration make the TLV170x family flexible enough to handle almost any application, from simple voltage detection to driving a single relay.

The TLV1701 is available in SC70-5, SOT23-5 and SOT553-5 packages. The TLV1702 is available in MSOP-8 and QFN-8 packages. The TLV1704 is available in a 14-pin TSSOP package.

All devices are specified for operation across the expanded industrial temperature range of –40°C to +125°C.

RELATED PRODUCTS

FEATURES	DEVICE
40-ns, 40-µA, push-pull comparator	TLV3201
	TLV3202
4.5-ns, rail-to-rail, push-pull, high-speed comparator	TLV3501
	TLV3502
Nanopower open-drain output comparator	TLV3401
	TLV3402
	TLV3404
3.9-µA, SC70-3 voltage reference	REF3325
	REF3330
	REF3333

(1) TLV1702 DGK package is production data. All other devices are product preview.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

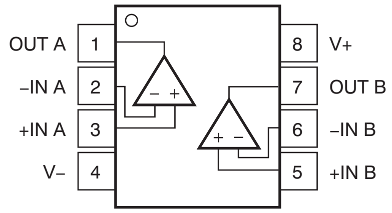
Over operating free-air temperature range, unless otherwise noted.

		VALUE	UNIT
Supply voltage		±20 (+40)	V
Signal input terminals	Voltage(2)	(V–) – 0.5 to (V+) + 0.5	V
	Current(2)	±10	mA
Output short-circuit(3)		Continous	mA
Operating temperature range		–55 to +150	°C
Storage temperature range, T_{stg}		–65 to +150	°C
Junction temperature, T_J		+150	°C
Electrostatic discharge (ESD) ratings	Human-body model (HBM)	2	kV
	Charged-device mode (CDM)	1.5	kV

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground; one comparator per package.

PIN CONFIGURATIONS

TLV1702: DGK PACKAGE
MSOP-8
(TOP VIEW)



NOTE: TLV1702 DGK package is production data. All other packages are product preview.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_S = +2.2 V to +36 V, C_L = 15 pF, R_{PULLUP} = 5.1 kΩ, V_{CM} = V_S / 2 and V_S = V_{PULLUP}, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input Offset voltage	TA = 25°C, V_S = 2.2 V		±0.5	±3.5	mV
		TA = 25°C, V_S = 36 V		±0.3	±2.5	mV
		T_A = –40°C to +125°C			±5.5	mV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C		±4	±20	μV/°C
PSRR	Power-supply rejection ratio			15	100	μV/V
		T_A = –40°C to +125°C		20		μV/V
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	T_A = –40°C to +125°C	(V–)		(V+)	V
INPUT BIAS CURRENT						
I_B	Input bias current			5	15	nA
		T_A = –40°C to +125°C			20	nA
I_{OS}	Input offset current			0.5		nA
C_{LOAD}	Capacitive load drive		See TYPICAL CHARACTERISTICS			
OUTPUT						
V_O	Voltage output swing from rail	I_O ≤ 4 mA, input overdrive = 100 mV, V_S = 36 V			900	mV
		I_O = 0 mA, input overdrive = 100 mV, V_S = 36 V			600	mV
I_{SC}	Short circuit sink current			20		mA
	Output leakage current	$V_{IN+} > V_{IN–}$		70		nA
SWITCHING CHARACTERISTICS						
t_{PHL}	Propagation delay time, high-to-low	Input overdrive = 100 mV		480		ns
t_{PLH}	Propagation delay time, low-to-high	Input overdrive = 100 mV		780		ns
t_R	Rise time	Input overdrive = 100 mV		2000		ns
t_F	Fall time	Input overdrive = 100 mV		400		ns
POWER SUPPLY						
V_S	Specified voltage range		2.2		36	V
I_Q	Quiescent current (per channel)	I_O = 0 A		55	75	μA
		I_O = 0 A, T_A = –40°C to +125°C			100	μA
TEMPERATURE						
	Specified range		–40		+125	°C
	Operating range		–55		+150	°C
	Storage range		–65		+150	°C

THERMAL INFORMATION

THERMAL METRIC[1]		TLV1702	UNITS
		DGK (MSOP)	
		8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	199	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	89.5	
θ_{JB}	Junction-to-board thermal resistance	120.4	
ψ_{JT}	Junction-to-top characterization parameter	22.0	
ψ_{JB}	Junction-to-board characterization parameter	118.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_{CC} = +5 V, $R_{PULL\text{-}UP}$ = 5.1 kΩ, and input overdrive = 100 mV, unless otherwise noted.

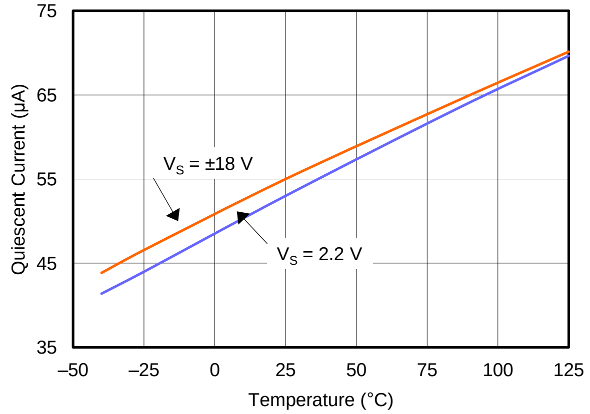


Figure 1. QUIESCENT CURRENT vs SUPPLY VOLTAGE

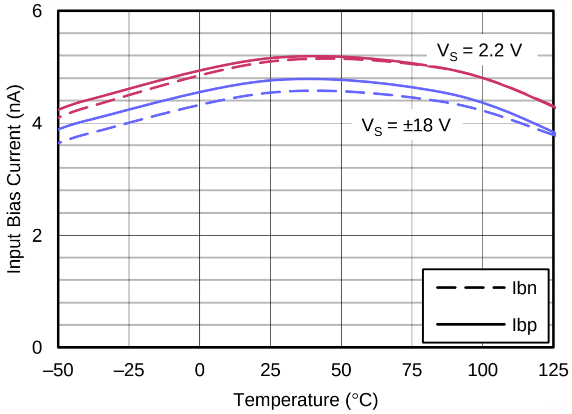


Figure 2. INPUT BIAS CURRENT vs TEMPERATURE

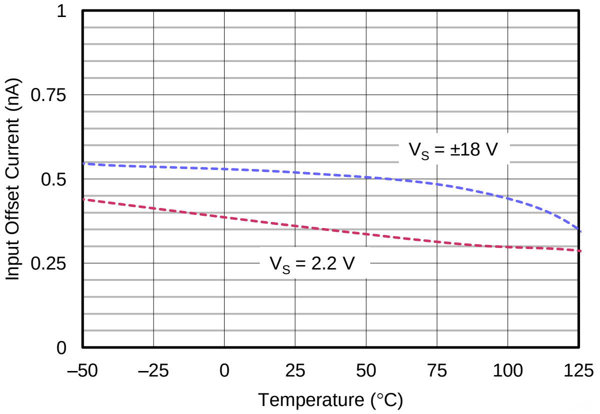


Figure 3. INPUT OFFSET CURRENT vs TEMPERATURE

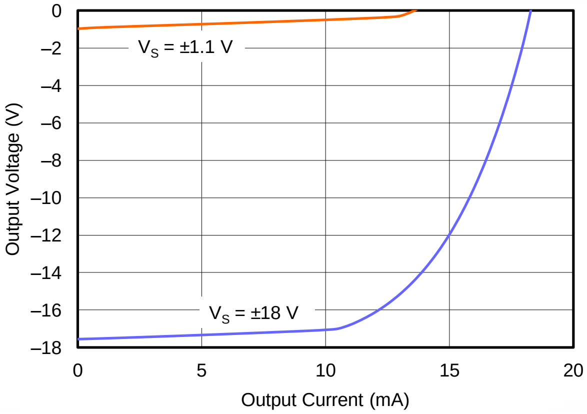


Figure 4. OUTPUT VOLTAGE vs OUTPUT CURRENT

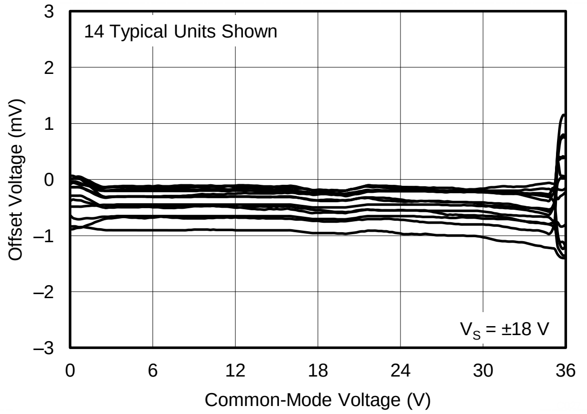


Figure 5. OFFSET VOLTAGE vs COMMON-MODE VOLTAGE (V_S = ±18 V)

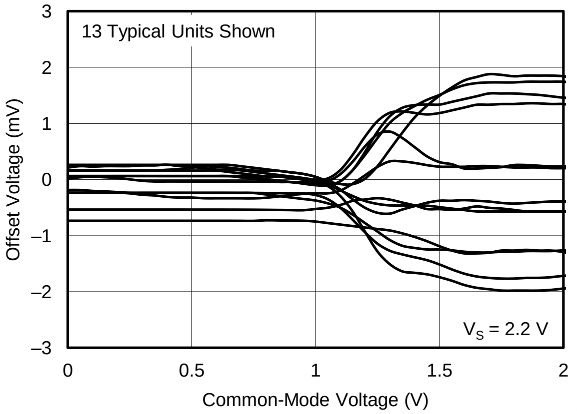


Figure 6. OFFSET VOLTAGE vs COMMON-MODE VOLTAGE (V_S = 2.2 V)

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CC} = +5 V, $R_{PULL\text{-}UP}$ = 5.1 kΩ, and input overdrive = 100 mV, unless otherwise noted.

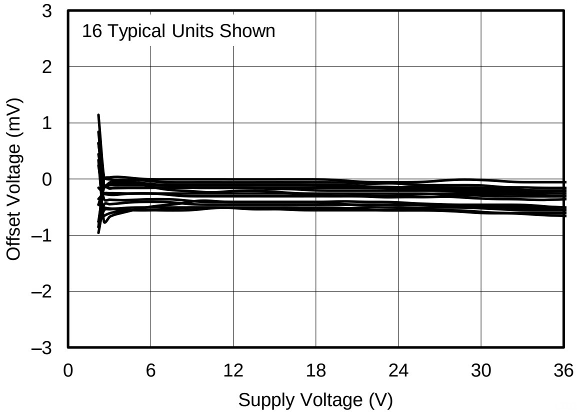


Figure 7. OFFSET VOLTAGE vs SUPPLY VOLTAGE

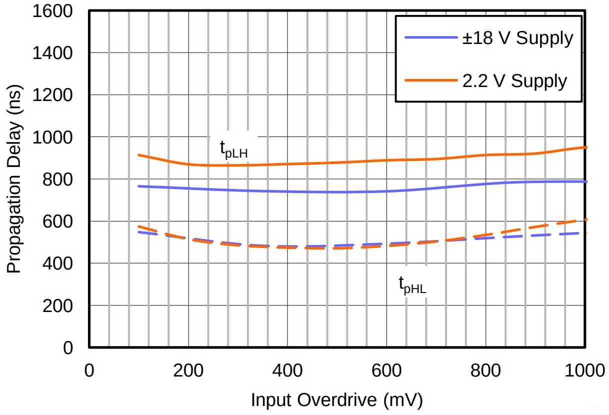


Figure 8. PROPAGATION DELAY vs INPUT OVERDRIVE

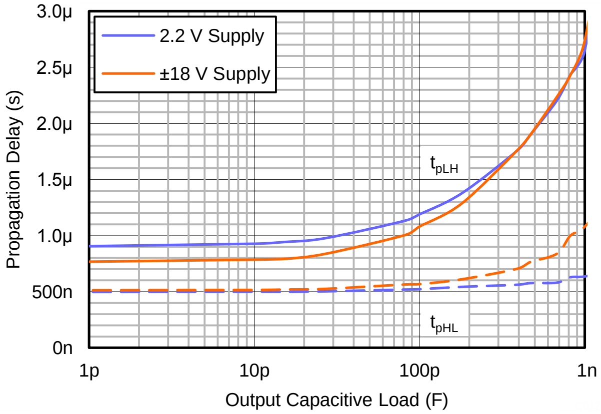


Figure 9. PROPAGATION DELAY vs CAPACITIVE LOAD

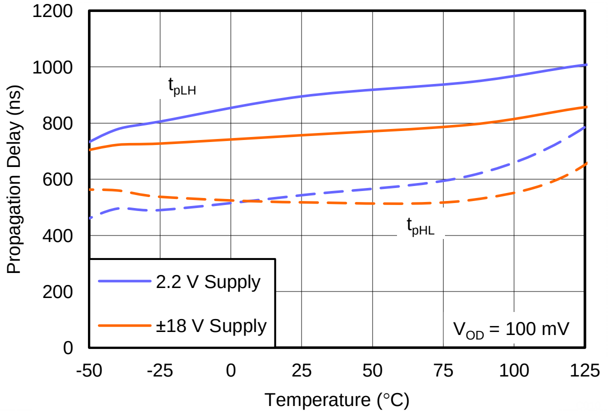


Figure 10. PROPAGATION DELAY vs TEMPERATURE

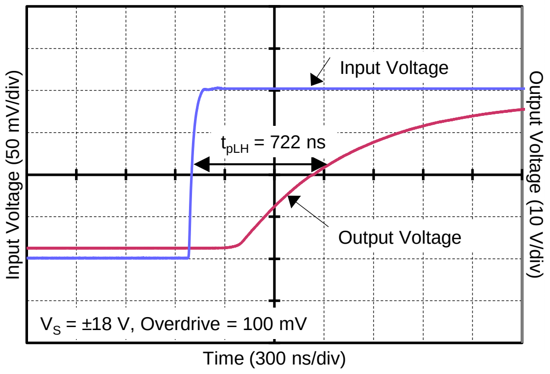


Figure 11. PROPAGATION DELAY (t_{pLH})
(V_S = ±18 V, Overdrive = 100 mV)

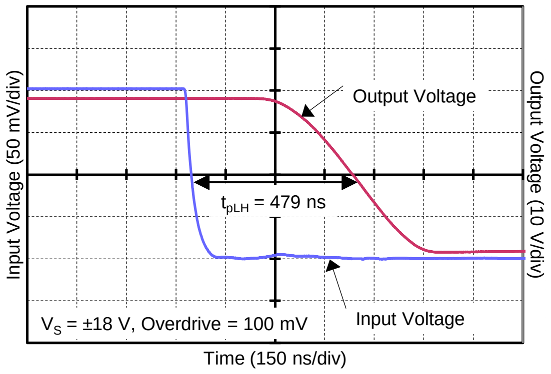


Figure 12. PROPAGATION DELAY (t_{pHL})
(V_S = ±18 V, Overdrive = 100 mV)

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CC} = +5 V, $R_{PULL\text{-}UP}$ = 5.1 kΩ, and input overdrive = 100 mV, unless otherwise noted.

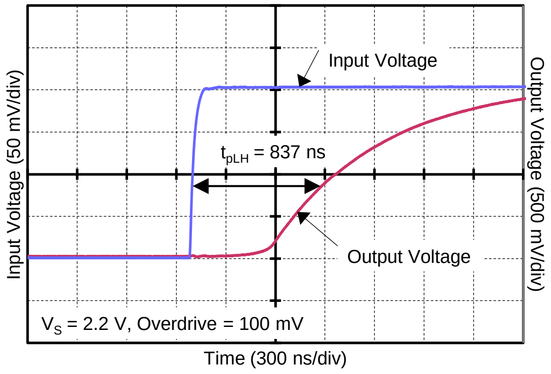


**Figure 13. PROPAGATION DELAY (t_{pLH})
(V_S = 2.2 V, Overdrive = 100 mV)**

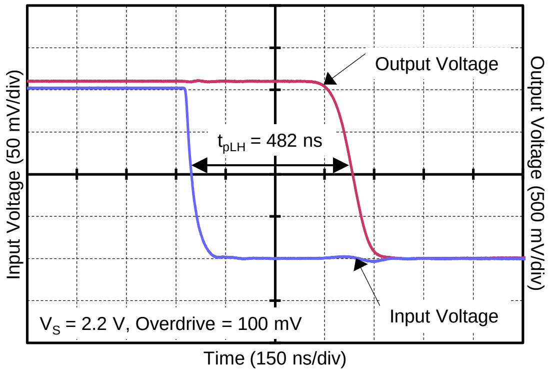


**Figure 14. PROPAGATION DELAY (t_{pHL})
(V_S = 2.2 V, Overdrive = 100 mV)**

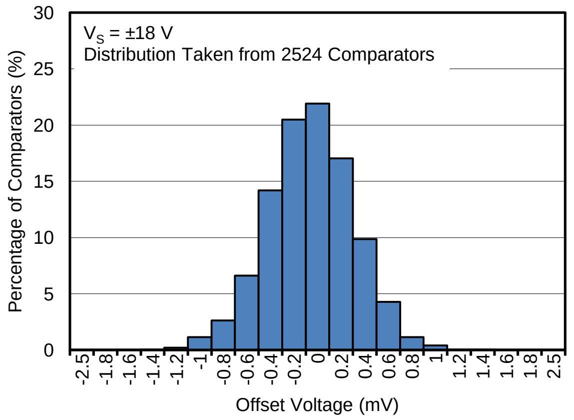


**Figure 15. OFFSET VOLTAGE PRODUCTION DISTRIBUTION
(V_S = ±18 V)**

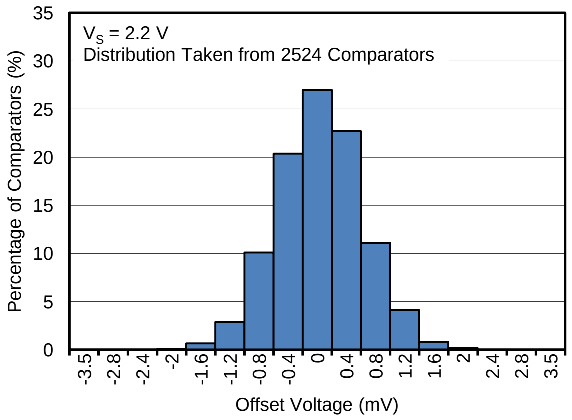


**Figure 16. OFFSET VOLTAGE PRODUCTION DISTRIBUTION
(V_S = 2.2 V)**

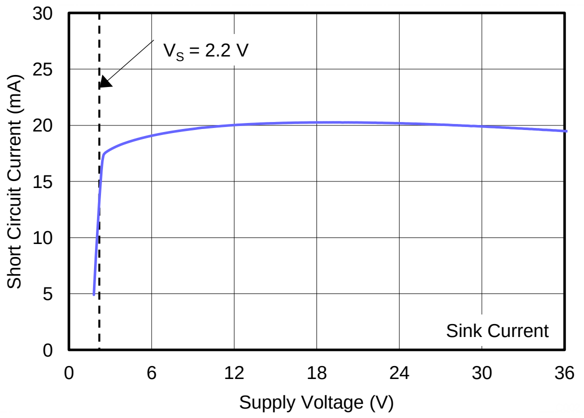


Figure 17. SHORT-CIRCUIT CURRENT vs SUPPLY VOLTAGE

APPLICATION INFORMATION

GENERAL DESCRIPTION

The TLV170x comparators features rail-to-rail input and output on supply voltages as high as 36 V. The rail-to-rail input stage enables detection of signals close to the supply and ground. The open collector configuration allows the device to be used in wired-OR configurations such as window comparator. A low supply current of 55 µA/channel with small, space-saving packages, makes these comparators versatile for use in a wide range of applications, from portable to industrial.

COMPARATOR INPUTS

The TLV170x are rail-to-rail input comparators, with an input common-mode range that includes the supply rails. The TLV170x is designed to prevent phase inversion when the input pins exceed the supply voltage. Figure 18 shows the TLV170x response when input voltages exceed the supply, resulting in no phase inversion.

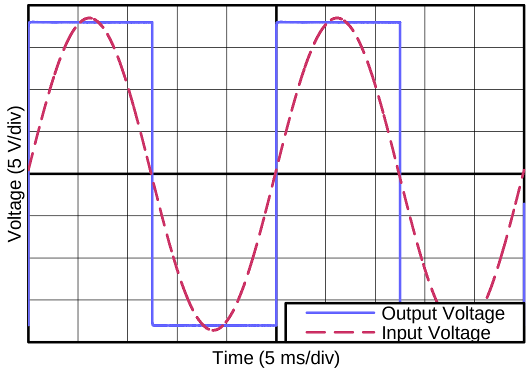


Figure 18. No Phase Inversion: Comparator Response to Input Voltage (Propagation Delay Included)

CIRCUIT LAYOUT

Comparators are very sensitive to input noise. For best results, the following layout guidelines should be maintained:

1. Use a printed circuit board (PCB) with a good, unbroken low-inductance ground plane. Proper grounding (use of ground plane) will help maintain specified performance of the TLV170x.
2. To minimize supply noise, place a decoupling capacitor (0.1-µF ceramic, surface-mount capacitor) as close as possible to V_{CC}.
3. On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
4. Solder the device directly to the PCB rather than using a socket.
5. For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. The topside ground plane runs between the output and inputs.
6. The ground pin ground trace runs under the device up to the bypass capacitor, shielding the inputs from the outputs.

SETTING REFERENCE VOLTAGE

It is important to use a stable reference when setting the transition point for the TLV170x. The REF3333 as shown in Figure 19 provides a 3.3-V reference voltage with low drift and only 3.9 µA of quiescent current.

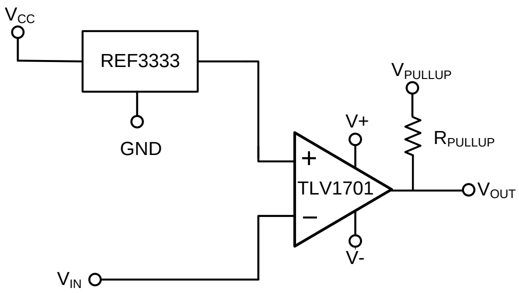
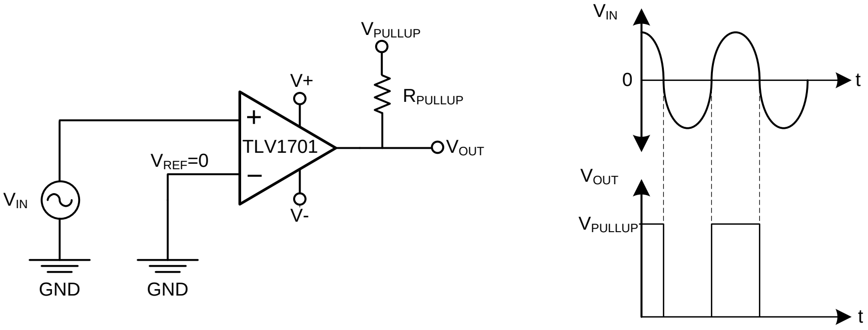


Figure 19. Reference Voltage for TLV170x

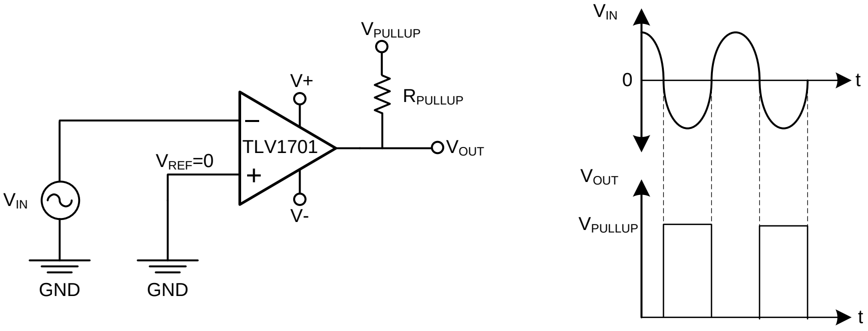
APPLICATION EXAMPLES

Application exmaples are shown in Figure 20 to Figure 23.

Zero Crossing Detector



(A) NON-INVERTING ZERO CROSSING DETECTOR



(B) INVERTING ZERO CROSSING DETECTOR

Figure 20. Zero Crossing Detector

Window Comparator

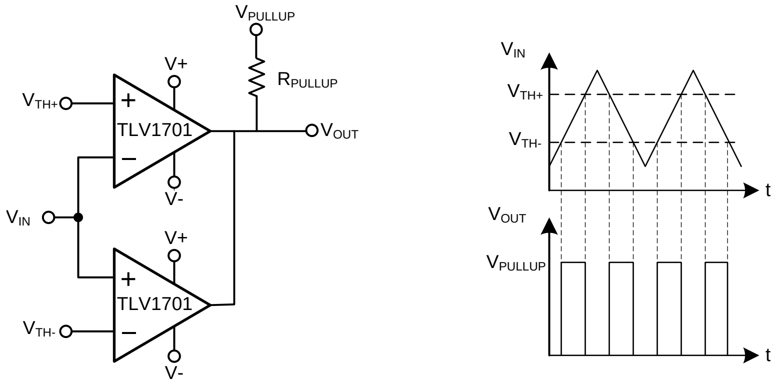


Figure 21. Window Comparator

Over and Undervoltage Detection

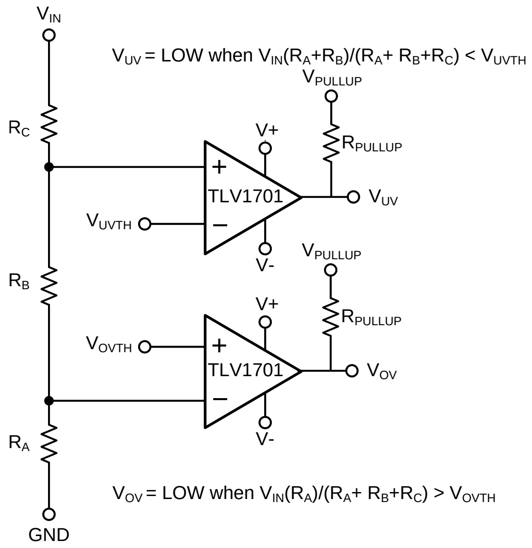


Figure 22. Over and Undervoltage Detection

High-Side Voltage Sense Circuit

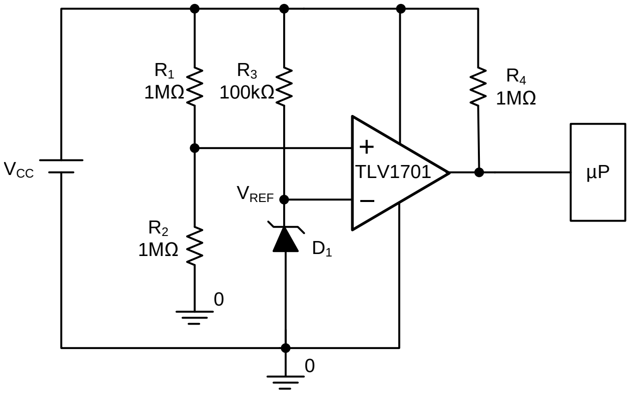


Figure 23. High-Side Voltage Sense Circuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV1702AIDGK	ACTIVE	VSSOP	DGK	8	80	TBD	Call TI	Call TI	-40 to 125		Samples
TLV1702AIDGKR	ACTIVE	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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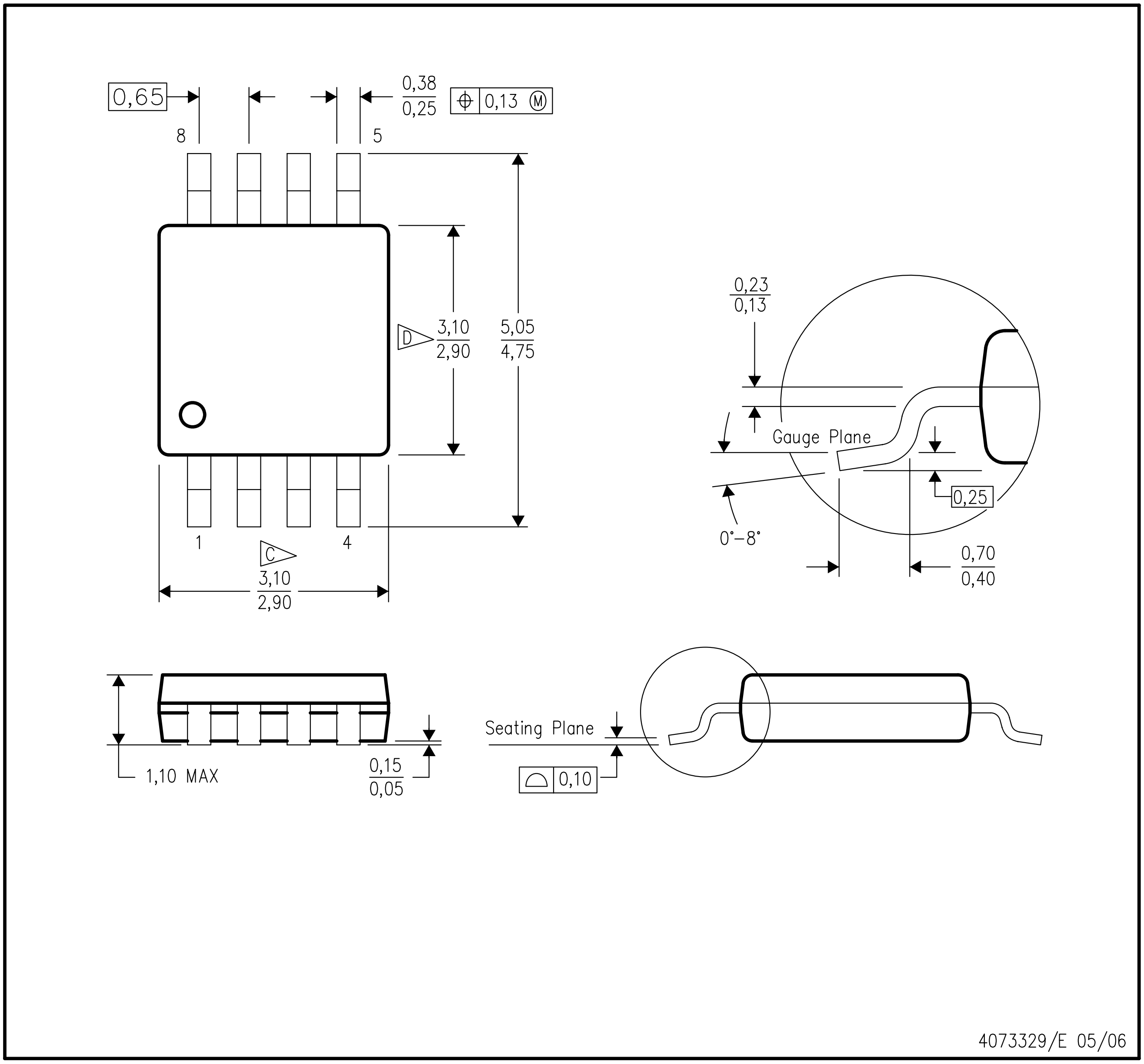
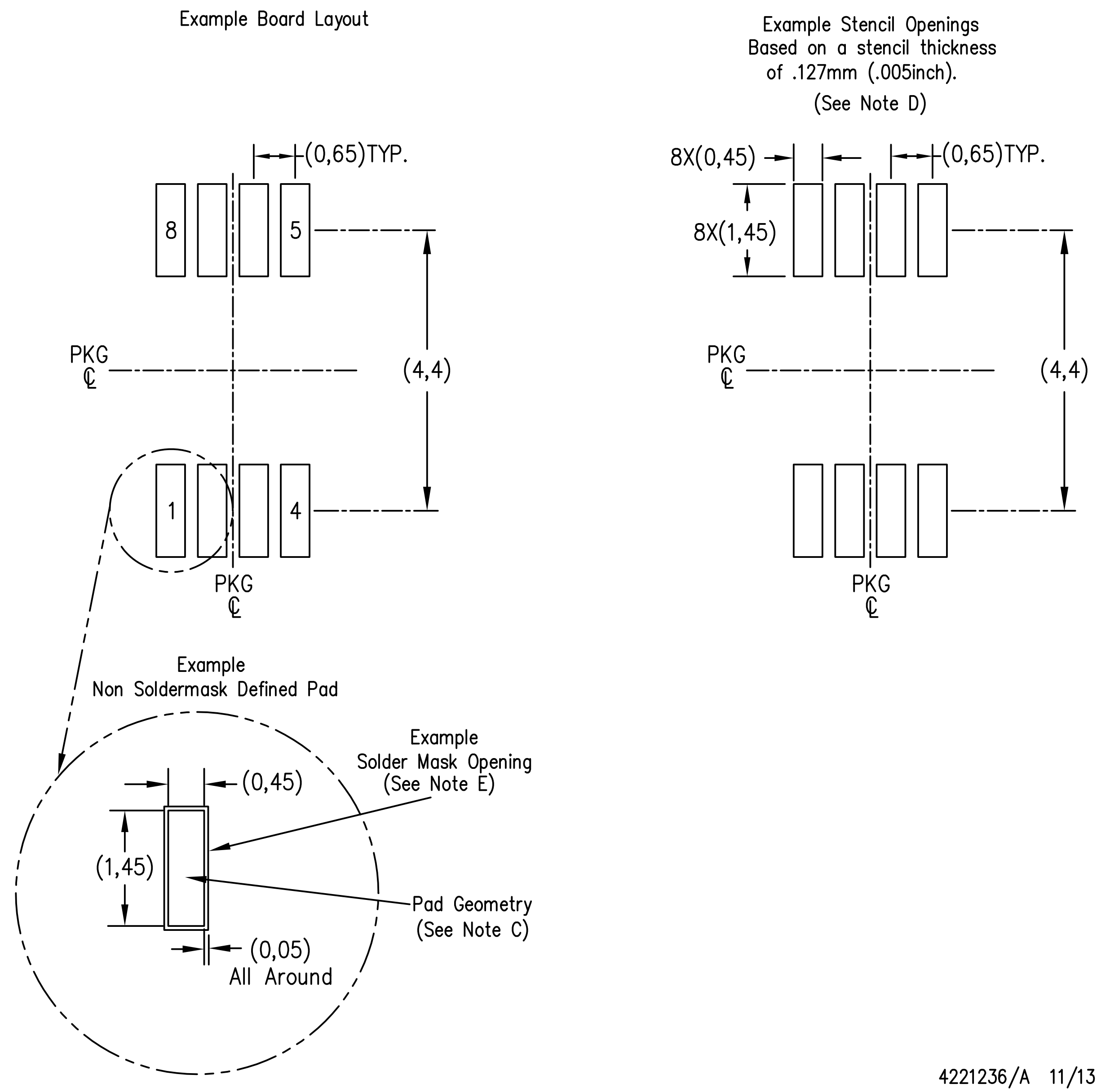
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



4221236/A 11/13

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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